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Kenton R. Mullins
Stout, Uxa, Buyan & Mullins, LLP
Suite 300
4 Venture
Irvine, CA 92618

EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	PAPER NUMBER
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/609,038	TSENG ET AL.	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2003 and 29 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 14-22* is/are rejected.

7)☒ Claim(s) *11-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09292003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to because Figs. 3-5 and 7A-8B have portions of the graphs that cannot be seen, or seen clearly. For example, see Fig 3 ("la" related section); 4 ("lb" related sections); 5 (bottom section); 7A (top three sections); 7B (middle two sections); the top two sections, and the bottom section, of both Figs. 7C and 8B; and 8A (top and bottom two sections). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: It is believed the references to "source" and "drain" on lines 9-12 of page 10 are reversed. Therefore, clarification and/or appropriate corrections are required.

Claim Objections

Claims 3, 7-8, and 10-22 are objected to because of the following informalities: Line 2 of both claims 3 and 16 should have "a supply" changed to --the supply-- since the "supply signal" was previously identified within the claims' respective independent claim. For similar reasons, "a supply" on line 3 of each of claims 7, 19, and 20 should be --the supply--. Claim 8, line 4 "a" should be --the-- (e.g. see "power-down mode" on line 3), and the extra period should be deleted at the end of the line. Claim 10, line 6 "a reset" should be --the reset-- to clearly relate back to "a reset signal" recited within the preamble. Since "a first threshold level" was already identified on line 6 of claim 10, it is suggested "a first" on lines 8-9 of claim 10 be changed to --the first--. For similar reasons, it is suggested "a reference" (lines 3 and 5), "a first" line (3), and "an increase" (lines 3-4) of claim 11 be changed to the article --the--. Claim 11, line 6 "an decrease" should be --a decrease-- to improve word flow. Claim 13, line 6 "a compensation" should be --the compensation-- (e.g. see "a compensation current" in line 5). The last line of claim 14 should have the extra period deleted. Similar to claim 11 above, "a ground" (lines 2-3 and 4), " a first" (line 3), "a supply" (line 3), "a power-up" (line 3), and "a power-down" (line 5) in claim 21 should use the article --the-- to minimize possible confusion. Claim 22, line 3 "a supply" should be --the supply--. Dependent claims carry over any objection(s) from any claim(s) upon which they depend. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-9, and 14-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. It is not clear what the "one V_t" in each of claims 1 (line 2) and 14 (line 7) represents. For example, does "one V_t" mean the Schmitt trigger circuit, the plurality of MOS devices, or each MOS device, has only "one V_t"? In line 2 of each of claims 2 and 15, "a small reset pulse" is vague and indefinite. For example, a pulse can have a small amplitude and/or pulse width with respect to any pulse that is larger. In claims 4 and 17, what is considered a "large low-side resistor"? For example, any resistor can be considered large with respect to any resistor that is smaller, even if the smaller resistor is not in the circuit, and any resistor coupled to a lower voltage than an element above it can be considered a low-side resistor. It is not clear in claim 21 if "a reset signal node" is referring to the same "reset signal node" in claim 20, or if two separate nodes are meant.

Claims 2 and 15 are each rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are how the compensate circuit and small reset pulse relate to the Schmitt trigger circuit and voltage divider recited within respective claim 1 or 14.

Dependent claims carry over any rejection(s) from any claim(s) upon which they depend.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 10, and in so far as being understood claims 1-2, 4-5, and 7-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Smith et al. (Smith). Fig. 3 shows a power-on reset circuit comprising Schmitt trigger circuit 46 and voltage divider 51,50,44 connected to input 52 of Schmitt trigger circuit 46. Fig. 8 shows an example of Schmitt trigger circuit 46 comprising a plurality of MOS devices, wherein one of ordinary skill in the art understands the devices determine the power reset trigger level. Using Fig 10 as a reference, reset signal 88 transitions from a low to high level once the power supply (represented by the solid "86,88" line) has reached a power-up threshold greater than midpoint 92 of the nominal power supply voltage range, and reset signal 88 transitions from a high to a low level once the power supply has decreased below a power-down threshold that is less than midpoint 92 (e.g. see column 10, lines 28-43). Section 51 of voltage divider 51,50,44 provides signals trgrdn and trgrup, which track (e.g. are proportional to) supply signal VDD (e.g. see columns 6 (lines 38-41) and 7 (lines 710)). Therefore, claim 1 is anticipated. Fig. 4 shows a temperature and voltage compensated reference generator circuit 62 (e.g. see column 7, lines 47-51) that provides its signal vref to voltage divider section 44. Deeming the Fig. 4 circuit as a compensate circuit that generates a small

reset pulse (e.g. the reference voltage) that compensates for temperature and supply signal variations, claim 2 is anticipated. Low-side resistor R5 is larger than resistor R4 (e.g. see column 7, lines 21-22), and this larger size can help reduce any leakage (e.g. unnecessary) current, thus anticipating claim 4. When the compensate circuit of Fig. 4 is considered to be part of the voltage divider, it effectively adjusts a feedback current (e.g. via 54, 50, 60, and 52) to help restore (e.g. maintain) voltage pupdn at input 52 of Schmitt trigger circuit 46, and claim 5 is anticipated. Referring to Figs. 3 and 11, Schmitt trigger circuit 46 has reset signal node 54 that provides a reset signal 88 (e.g. pwrenb) that rises from ground potential (e.g. a logic low) to a first voltage (e.g. a logic high) when supply signal 86 has increased enough to favorably compare to a first threshold voltage 96 (e.g. signal 86 > voltage 96); and reset signal node 54 drops from the first voltage to the ground potential when supply signal 86 does not compare favorably to the first threshold voltage 96 (e.g. voltage 98 < voltage 96). Since the Smith reference does not clearly show or disclose a sleep mode, one of ordinary skill in the art would consider Smith's power-on reset circuit' operation corresponds to the normal operation of a power-on reset circuit that includes power-up and power-down modes, but does not include a sleep mode. Without a sleep mode, the circuit does not enter into it, and claim 7 is anticipated. Interpreting Fig. 11 in a slightly different manner, and also referring to Fig. 10, one of ordinary skill in the art would understand Schmitt trigger circuit 46 has a first voltage peak (e.g. 98 of Fig. 11 corresponds to the power-down threshold level shown in Fig. 10 that is represented by the intersection of lines 88 and 86 shown below 92), and a second voltage peak (e.g. 96 of Fig. 11 corresponds to the power-up threshold level shown in Fig. 10 that is represented by the intersection of lines 86 and 88 shown above 92). Since 98 corresponds to when Schmitt trigger circuit 46 enters a power-

down mode, and 96 corresponds to when Schmitt trigger circuit 46 exits the power-down mode (e.g. returns to a normal, active operation), claim 8 is anticipated because second voltage peak 96 is greater than first voltage peak 98. Interpreting the figures in yet another way, Smith's reference shows a method for providing a reset signal in response to a supply signal. This method comprises: generating a primary current within 51 in response to the supply signal; generating a trigger voltage trgrdn/trgrup in response to the primary current; if supply signal 86 does not compare favorably to first threshold level (e.g. it's not below 96, which is not lower than 98) reset signal 88 is increased from a reference potential (i.e. logic low) to a first potential (i.e. logic high) in response to an increase of supply signal 86; and if supply signal 86 compares favorably to first threshold level 98 (i.e. it's lower than 98), the reset signal 88 is set to the reference potential. Therefore, claim 10 is anticipated. [Note: Smith's circuit does not enter the sleep mode because it is assumed it operates only in the power-up and power-down modes.]

Claim 10 is rejected under 35 U.S.C. 102(e) as being anticipated by Slamowitz et al. (Slamowitz). The Fig 4 power-on reset circuit 400 of Slamowitz is understood as a method for providing a reset signal (e.g. schmit_out) in response to supply signal vddc. The method comprises 434,414 generating a primary current in response to supply signal vddc; 416,418 generating trigger voltage V1,V2 in response to the primary current; if supply signal vddc does not compare favorably to a first threshold level (e.g. not being below power-up threshold level, that is greater than the first (power-down) threshold level), the reset signal is increased from a reference potential (e.g. logic low) to a first potential (e.g. logic high) in response to the supply signal increase; and if supply signal vddc compares favorably to the first threshold level (e.g. less

than the power-down threshold level), the reset signal is set to the reference potential, thus rendering claim 10 obvious.

Claim Rejections - 35 USC § 102/103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Smith et al. (Smith) as applied to claim 1 above. As previously described, Smith shows a power-on reset circuit comprising Schmitt trigger circuit 46 and voltage divider 51,50,44. Voltage divider section 44 is shown in Fig. 7 comprising current source transistors M15 and M18 which will generate current in response to the supply signal, thus anticipating claim 3. However, voltage divider section 51 can be modified to include a current source transistor. For example, it would have been obvious to one of ordinary skill in the art to replace at least one of resistors R3-R5 with a corresponding transistor receiving a respective bias voltage to control its resistance. Each transistor can be deemed a current source transistor that will generate current (e.g. allow current to flow through it) in response to the supply signal, thus rendering claim 3 obvious. By replacing at least one of resistors R3-R5 with a transistor, the trigger voltages trgrdn and trgrup can be adjusted to desired levels. For example, perhaps the power-up level is not what was initially expected. Therefore, if voltage divider section 51 has at least one (current source) transistor within its current path, the power-up level can be adjusted by changing the bias voltage to the transistor(s) to meet a required level. The

more resistors that are replaced by a corresponding transistor, the more accurate the trigger levels can be set after fabrication.

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

In so far as being understood, claims 1-5, 7-8, and 14-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Slamowitz et al. (Slamowitz), in view of Smith et al. (Smith). Fig. 4 of Slamowitz shows a power-on reset circuit comprising Schmitt trigger circuit 442 for determining a power reset trigger level of signal schmit_out; and voltage divider circuit 410,412 is connected to the input of Schmitt trigger circuit 442. As shown in Fig. 5, and understood by one of ordinary skill in the art, voltage divider section 412 tracks supply signal Vddc. However, the reference of Slamowitz does not show or disclose Schmitt trigger circuit 442 constructed with a plurality of MOS devices, or wherein the power-on reset circuit is within a computer

system that comprises a microprocessor, bus, and memory. Fig. 8 of Smith shows Schmitt trigger circuit 46 comprising a plurality of MOS devices M20-M23. Therefore, it would have been obvious to one of ordinary skill in the art to replace Slamowitz's Schmitt trigger circuit 442 with Smith's Schmitt trigger circuit 46. Since one of ordinary skill in the art knows a Schmitt trigger has a power-up threshold higher than its power-down threshold, with respect to the power reset trigger level, the Slamowitz/Smith configuration renders claim 1 obvious. 438 can be considered one type of a compensate circuit to compensate for temperature and supply signal variations (e.g. see paragraph 0042, wherein it is understood that changes in temperature can also affect and/or cause power supply type changes). The on/off operation of 438 will generate what can be deemed a small reset pulse, thus rendering claim 2 obvious. Voltage divider section 412 includes current source transistors 434 and 414, which generate a current in response to supply signal vddc, and claim 3 is rendered obvious. Referring to a resistor divider circuit, paragraphs 0012 and 0039 both indicate the series resistors can have different resistance values. Therefore, when resistors 416 and 418 are of different values, the large one can be considered a "large low-side resistor" (e.g. both resistors are coupled between 414 and low side gndd). Since both resistors limit the current flowing through the series path of 434,414,416,418, each one effectively reduces leakage (e.g. unnecessary) current, rendering claim 4 obvious. Transistor 438, included in voltage divider 410,412, provides one type of compensate circuit that adjusts a feedback current to help restore (e.g. maintain) the voltage at the input of Schmitt trigger circuit 442 in response to supply signal fluctuations (e.g. see paragraph 0042, wherein one of ordinary skill in the art would understand the phrase "prevent false re-triggering" is one way of stating the signal is not changed enough to cause inaccurate triggering of the power-on reset circuit).

Therefore, claim 5 is rendered obvious. Since the Slamowitz/Smith configuration is understood to operate as a power-on reset circuit with power-up and power-down modes, it will not enter a sleep mode. Therefore, one of ordinary skill in the art will understand that the Schmitt trigger circuit will comprise a reset signal node that has a signal that will rise from a ground potential (e.g. a logic low) to a first voltage (e.g. a logic high) as the supply signal increases and it compares favorably with a first threshold voltage (e.g. it's equal to, or greater than, the power-up threshold). Also, the signal at the reset signal node will drop from the first voltage to the ground potential when the supply signal does not compare favorably to the first threshold voltage (e.g. it's below the first threshold voltage by a predetermined amount), thus rendering claim 7 obvious. Understanding the operation of a Schmitt trigger circuit, one of ordinary skill in the art will understand that the signal on a reset signal node has a first voltage peak (e.g. power-down threshold level) when the Schmitt trigger circuit enters a power-down mode, and a second voltage peak (e.g. power-up threshold level), greater than the first voltage peak, when the Schmitt trigger circuit exits the power-down mode (e.g. enters the active mode). Therefore, claim 8 is rendered obvious. It also would have been obvious to one of ordinary skill in the art to use the Slamowitz/Smith power-on reset circuit within a computer system comprising a microprocessor coupled to a memory by a bus, wherein the power-on reset circuit would generate a power-on reset signal to the microprocessor. Computer systems typically comprise some type of a power-on reset circuit to ensure the power supply circuit has reached at least a minimum acceptable voltage level that will ensure the system will operate properly. This use is considered one known and intended use for a power-on reset circuit by the examiner. By letting the computer's processor know when the power supply is within, or below, its acceptable limits,

the power-on reset circuit can minimize inaccurate operations of the computer system. Other than the additional computer system, microprocessor, bus, and memory limitations recited within independent claim 14, the power-on reset circuit limitations of claims 14-17 and 19 correspond to the limitations recited in claims 1-4 and 7, respectively. Therefore, claims 14-17 and 19 are rendered obvious for the same reasons as described above with respect to the rejections of claims 1-4 and 7. Although claim 18 closely corresponds to claim 5, claim 18 recites "in response to a fluctuation in temperature", wherein claim 5 recites "in response to a fluctuation in the supply signal." However, it would have been obvious to one of ordinary skill in the art to consider that 438 can function as one type of a compensate circuit that adjusts feedback current in response to temperature fluctuations, because it is understood that changes in temperature can also affect supply signal levels. Since 438 provides hysteresis to help prevent false re-triggering in the presence of power supply fluctuations (e.g. see paragraph 0042), 438 can also help compensate for temperature fluctuations that affect the power supply. Therefore, claim 18 is rendered obvious.

No claim is allowable as presently written.

Allowable Subject Matter

Claims 11-13 are only objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However, claims 11 and 13 each have their own respective objections which should be addressed and corrected, and each of claims 11-13 carry over the objection(s) from claim 10. There is presently no motivation to modify or combine any prior art reference(s) to ensure the method steps also include the increase to the first/second potential in

response to the supply signal when a power-up/power-down state is respectively entered as recited within claim 11, upon which claims 12-13 depend.

Also, claims 6, 9, and 20-22 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. There is presently no motivation to modify or combine any prior art reference(s) to ensure: 1) the Schmitt trigger circuit has the first/second voltages with respect to the power-down/sleep modes as recited within claim 6; 2) the reset signal node of the Schmitt trigger circuit has a third voltage with respect to a sleep mode as recited within claim 9; 3) the specific relationships with respect to the rising of the first voltage and the power-up, power-down, and sleep modes are recited within claim 20 (upon which claim 21 depends; and 4) similar to claim 6 described above, the rising of the first/second voltages with respect to the power-up/power-down modes as recited within claim 22.

Prior Art

The other prior art reference cited on the accompanying PTO-892 is deemed relevant to at least sections of the claimed invention. Although not used in any formal prior art rejection described above, the reference of Dasgupta reads on the basic limitations recited within at least claims 1 and 3. For example, Fig. 1 shows a power-on reset circuit comprising Schmitt trigger circuit 13 (e.g. see column 3, lines 25-28) constructed with a plurality of MOS devices, and voltage divider 11,12 connected to input n4 of Schmitt trigger circuit 13, wherein the voltage divider effectively tracks supply signal VDD (e.g. see Curve1 and Curve 3 in Fig. 2). Most, if not all, of the transistors within voltage divider 11,12 can be considered one type of current source. It is also noted that the elements within Schmitt trigger circuit 13 closely correspond to

elements M10-M12,M14,M16-M17 shown in the applicants' own Fig. 2 Schmitt trigger circuit 30/first inverter X1. Dasgupta also relates the power-on reset circuit to memories (e.g. see columns 1 (lines 16-18) and 3 (lines 49-51)). Therefore, this reference should be carefully reviewed and considered with respect to at least the basic claim limitations (i.e. Schmitt trigger circuit and voltage divider).

The prior art reference cited on the IDS submitted Sep 29, 2003 was reviewed and considered. This reference does not clearly disclose a Schmitt trigger (e.g. Schmidt trigger, or even hysteresis), or even the entering into a sleep (e.g. idle or standby) type mode recited within some of the claims.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund
28 September 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800